Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(use as many sheets as necessary)*	**Complete if Known**	
	Application Number	10/037,593
	Filing Date	October 19, 2001
	First Named Inventor	Matthew P. Kulig
	Art Unit	2157
	Examiner Name	Barbara N. Burgess
Sheet 1 of 6	Attorney Docket Number	60022210-0157

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number — Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	IN	US 2001/0056547 A1	12-27-2001	Dixon	
	IO	US 2003/0009693 A1	01-03-2003	Brock et al.	
	IP	US 2003/0014662 A1	01-16-2003	Gupta et al.	
	IQ	US 2003/0051043 A1	03-13-2003	Wyschogrod et al.	
	IR	US 2003/0074582 A1	04-17-2003	Patel et al.	
	IS	US 5,347,634	09-09-1994	Herrell et al	
	IT	US 5,371,794	12-06-1994	Diffie et al.	
	IU	US 5,421,028	05-30-1995	Swanson	
	IV	US 6,028,939	02-22-2000	Yin	
	IW	US 6,389,532 B1	05-14-2002	Gupta et al.	
	IX	US 6,804,667 B1	10-12-2004	Martin	
	IY	US 7,127,510 B1	10-24-2006	Yoda et al.	

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number — Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Notices of Allowance mailed:
	0046	US 2005/0086520 A1	04/21/2005	Dharmapurikar et al.	07/09/2008

Examiner Signature	/Barbara Burgess/	Date Considered	02/12/2009

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.B./

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	Examiner Name	Barbara N. Burgess
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Number — Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	IZ	EP 0 573 991 B1	01-16-2002	Cantor Fitzgerald		
	JA	JP 9-269930	10-14-1997	Hitachi Ltd.		
	JB	JP 10-313341	11-24-1998	Nat'l Aerospace Lab Kagaku Gijutsu Shinko Jigyodan		
	JC	JP 2000-357176	12-26-2000	IBM		
	JD	JP 2001-014239	01-19-2001	Hitachi Ltd.		
	JE	JP 2001-217834	10-08-2001	IBM		
	JF	JP 2001-518724	10-16-2001	Worldtalk Corporation		
	JG	WO 90/010910 A1	09-20-1990	Chicago Board of Trade		
	JH	WO 97/377735 A1	10-16-1997	ORIS, LLC		
	JI	WO 99/05814 A2	02-04-1999	Worldtalk Corporation		
	JJ	WO 99/55052 A1	10-28-1999	Sun Microsystems, Inc.		
	JK	WO 01/39577 A1	06-07-2001	Nokia Mobile Phones Ltd.		
	JL	WO 03/036845 A2	05-01-2003	Global Velocity		

Examiner Signature	/Barbara Burgess/	Date Considered	02/12/2009

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.B./

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	Group Art Unit	2157
	Examiner Name	Barbara N. Burgess
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OTHER ITEMS – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	JM	ANONYMOUS, "Method for Allocating Computer Disk Space to a File of Known Size", IBM Technical Disclosure Bulletin, Vol. 27, No. 10B, New York, NY, March 1. 1985.	
	JN	ARNOLD, Jeffrey et al., "The Splash 2 Processor and Applications", Proceedings 1993 IEEE International Conference on Computer Design: VLSI in Computers and Processors, October 3, 1993, pp. 482-485, Cambridge, Massachusetts.	
	JO	BAER, Jean-Loup, Computer Systems Architecture, pp. 262-265, Computer Science Press, Rockville, MD, 1980.	
	JP	BARONE-ASESI, G. & WHALEY, R., "Efficient Analytic Approximation of American Option Values", Journal of Finance, 42(2): 301-320, June 1987.	
	JQ	BOSSARDT, Matthias et al., "ABR Architecture and Simulation for an Input-Buffered and Per-VC Queued ATM Switch", IEEE Global Telecommunications Conference (Globecom'98), pages 1817-1822, Sydney, Australia, Nov. 1998.	
	JR	BRAUN, Florian et al., "Layered Protocol Wrappers for Internet Packet Processing in Reconfigurable Hardware", Washington University, Department of Computer Science, Technical Report WUCS-01-10, July, 2001, Proceedings of Hot Interconnects 9 (Hotl-9), Stanford, CA, Aug. 22-24, 2001, pp. 93-98.	
	JS	CHANEY, Tom et al., "Design of a Gigabit ATM Switch", Proceedings IEEE, 1:2-11, INFOCOM '97, Sixteenth Annual Joint Conference of the IEEE Computer and Communications Societies, April 7-11, 1997, Kobe, Japan.	
	JT	CHOI, Sumi et al., "Design of a Flexible Open Platform for High Performance Active Networks", (Presentation Slides) Allerton Conference, Champaign, IL, 1999.	
	JU	CONG, Jason & DING, Yuzheng, "An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs", IEEE/ACM International Conference on Computer-Aided Design, Santa Clara, CA, Digest of Technical Papers., pp. 48-53, November 8, 1992.	
	JV	DHARMAPURIKAR, Sarang et al., "Synthesizable Design of a Multi-Module Memory Controller", Washington University, Dept. of Computer Science, Technical Report WUCS-01-26, October 12, 2001.	

Examiner Signature	/Barbara Burgess/	Date Considered	02/12/2009

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.B./

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	JW	DUAN, Haoran et al., "A High-performance OC-12/OC-48 Queue Design Prototype for Input-buffered ATM Switches", IEEE Infocom '97, pp 20-28, Kobe, Japan, April 7-11, 1997.	
	JX	EBELING, Carl et al., "RaPiD - Reconfigurable Pipelined Datapath", FPL '96: The 6th International Workshop on Field Programmable Logic and Applications, Springer-Verlag, University of Washington, Dept. of Computer Science and Engineering, September 23, 1996, Seattle, WA.	
	JY	FELDMANN, Anja, "BLT: Bi-Layer Tracing of HTTP and TCP/IP", Computer Networks 33(1):321-335, June 2000.	
	JZ	GAVRILA, D.M., "Multi-feature Hierarchical Template Matching Using Distance Transforms", Proceedings of the 14th International Conference on Pattern Recognition, 1:439-444, Brisbane, Qld., AU, August 16-20, 1998.	
	KA	GUNTHER, Bernhard et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", IEEE, pp. 10-17, Proceedings, IEEE Symposium on FPGAs for Custom Computing Machines, Napa Valley, CA, April 17, 1996.	
	KB	HAYES, John P., Computer Architecture and Organization, Second Edition, 1988, pp. 448-459, McGraw-Hill, Inc., New York, NY, 1988.	
	KC	HORTA, Edson L. et al., "PARBIT: A Tool to Transform Bitfiles to Implement Partial Reconfiguration of Field Programmable Gate Arrays (FPGAs)", Washington University, Department of Computer Science, Technical Report WUCS-01-13, July 6, 2001.	
	KD	KUHNS, Fred et al., "Implementation of an Open Multi-Service Router", Washington University, Department of Computer Science, Technical Report WUCS-01-20, August 15, 2001.	
	KE	LIN, Ting-Pang et al., "Real-Time Image Template Matching Based on Systolic Amy Processor", International Journal of Electronics, December 1, 1992, pp. 11651 176, Vol. 73, No. 6, London, Great Britain.	
	KF	LOCKWOOD, John W., "Project History and Previous Research on the Illinois Input Queue and WUGS/iiQueue Integration, Aug. 1998.	
	KG	LOCKWOOD, John W., "Quality of Service Enhancement of Washington University Gigabit Switch Using the Illinois Input Queue, December 1996, Urbana and Champaign, IL.	

Examiner Signature	/Barbara Burgess/	Date Considered	02/12/2009

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.B./

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(use as many sheets as necessary)*				*Complete if Known*	
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	KH	LOCKWOOD, John William, "Design and Implementation of a Multicast, Input-Buffered ATM Switch for the iPOINT Testbed", PhD Dissertation, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, UMI Number: 9625160, 1995.	
	KI	MOSANYA, Emeka et at., "A FPGA-Based Hardware Implementation of Generalized Profile Search Using Online Arithmetic", ACMISIGDA International Symposium on Field Programmable Gate Arrays, February 21, 1999, pp. 101-111, Monterey, California	
	KJ	NUNEZ, Jose Louis et al., "The X-MatchLITE FPGA-Based Data Compressor", Euromicro Conference 1999, Proceedings, Italy, Sept. 8-10, 1999, Los Alamitos. CA	
	KK	RAMAKRISHNA, M.V. et al., "A Performance Study of Hashing Functions for Hardware Applications", Journal of Computing and Information, Vol. 1, No. 1, May 1994, pp. 1621-1636.	
	KL	RAMAKRISHNA, M.V. et al., "Efficient Hardware Hashing Functions for High Performance Computers", IEEE Transactions on Computers 46(12):1378-1381, December 1997.	
	KM	RATHA, Nalini K., et al., "Convolution on Splash 2", Proceedings of IEEE Symposium on FPGAs for Custom Computing Machines, pp. 204-213, Los Alamitos, California, April 19, 1995.	
	KN	REHMAN, Rafeeq Ur, HP-Certified HP-UX System Administration, Prentice Hall PTR, Indianapolis, IN, May 31, 2000, from: http://proquest.safaribooksonline.com/0130183741	
	KO	ROBERTS, Lawrence, "Internet Still Growing Dramatically Says Internet Founder", Press Release, Caspian Networks, Inc. -- Virtual Pressroom, PR Newswire, New York, NY, August 15, 2001.	
	KP	SCHMIT, Herman, "Incremental Reconfiguration for Pipelined Applications", IEEE, 47-55, Proceedings of the 5th Annual IEEE Symposium on FPGAs for Custom Computing Machines, April 1997, Dept. of ECE. Carnegie Mellon University, Pittsburgh, PA.	
	KQ	SHIRAZI, N. et al., "Quantitative Analysis of FPGA-Based Database Searching", Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology, May 2001, pp. 8596, Vol. 28, No. 112, Dordrecht, Netherlands	
	KR	TAYLOR, David et al., "Scalable IP Lookup for Programmable Routers", Washington University, Department of Computer Science, Technical Report WUCS-01-33, October 1, 2001.	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.B./

Substitute for form 1449B/PTO # INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				**Complete *if Known***	
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	KS	VILLASENOR, John et al., "Configurable Computing Solutions for Automatic Target Recognition", Proceedings of IEEE Symposium on FPGAs for Custom Computing Machines, April 17, 1996, pp. 70-79, Los Alamitos, California.	
	KT	WOOSTER, et al., "HTTPDUMP Network HTTP Packet Snooper", April 25,1996, available at http://ei.cs.vt.edu/~succeed/96httpdump/html/paper.html	

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